A Passive Inter Turn Short Circuit Fault Mitigation Technique for Electric Machines

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***Abstract*—This paper proposes a passive inter turn short circuit current mitigation technique that adds differential mode chokes (DMCs) between the inverter and the phase pairs in a multiphase winding arrangement. The fault current manifests itself as a differential mode current between faulted phases, and this paper shows that the DMCs can reduce the fault current, while the DMCs only slightly affect the common mode or healthy current. The amplitude of the fault current reduction depends on the DMC size. This study shows that a 200 μH DMC can reduce the fault current by multiple orders of magnitude from 4586% (without DMCs) to 10% of the rated current for a simulated permanent magnet synchronous machine. With that level of fault current mitigation, the machine can continue operating almost normally. A setup based on transformers cores was built and tested. The experimental results show that, with a 65 μH DMC, the fault current is reduced from 120% to less than 1% of the rated current. The good agreement between simulation and experimental results validates the model.**

***Index Terms*—short circuit fault current, mitigation technique, differential mode choke (DMC), fault tolerant design, reliability, permanent magnet machines, multiphase electric machines, winding arrangement.**

I. Introduction

DUE to their high torque density and high efficiency, surface mounted permanent magnet (SPM) machines are among the most popular choices for high performance applications like all-electric aircraft [1]–[3]. However, reliability plays a key role in such applications, so fault tolerant design is critical. Nowadays, the increasing switching frequencies enabled by Wide Band Gap (WBG) devices are increasing the dv/dt stresses on machine windings [4]. Additionally, high performance requirements are driving increasing temperatures in machines. These factors can reduce the insulation lifespan and increase the chances of inter-turn short circuit (ITSC) faults. This type of fault is particularly dangerous in SPM machines due to their low inductance [5]. In addition, the rotor permanent magnet (PM) excitation cannot be turned off, so the fault current will continue circulating in the machine until rotation ceases. Thus, the fault current could cause serious failures including demagnetization of the PMs or even fire [6]. Therefore, researchers have proposed various approaches to make the motor drive system more fault tolerant.

Some researchers have investigated the fault tolerant performance from a design or topology perspective. [7] has proposed an approach to select a certain combination of slots/poles for fault tolerant operation. This approach is based on minimizing the coupling between phases and also effectively eliminating low order MMF harmonics to reduce rotor stray flux and ovalizing vibration under normal operation. The authors of [8] have reviewed different approaches including modular design of both winding and stator, rotor structure, slot shape and slot opening, thermal and mechanical considerations to achieve fault tolerant operation. [9]–[13] have particularly focused on fault tolerant design of the motor drive system for safety critical applications like aerospace. Additionally, redundancy is a common way to make the drive system fault tolerant. For example, dual windings are proposed in [14], [15] to have a six phase machine. In case of any fault, the remaining healthy set of windings drives the motor, but the power is significantly reduced or the losses are significantly increased.

Some studies have investigated current injection as an effective method to mitigate the fault. In [16], it is shown that simplest fault ITSC fault mitigation method, shorting the phase terminals, is not an effective way to alleviate the ITSC fault current in large machines with bar wound windings. Therefore, a method based on current injection is proposed that can effectively decrease the short circuit fault current with 1 p.u current injection. Another current-injection-based fault tolerant control method is proposed in [17] to minimize the torque ripple caused by ITSC faults. The fault tolerant control is integrated into the Field Oriented Control (FOC) in order to keep the motor normally running and retain its torque capability. Another current injection scheme based on controlling the phase-angle of the normal phases current for a permanent magnet vernier machine is proposed in [18]. This strategy reduces the number of unknown quantities and, as a result, the computational burden. The normal torque is maintained and torque ripple is minimized. A global fault tolerant current injection technique to achieve a ripple free output torque with minimum copper loss based on a general closed-form solution or a numerical analysis are proposed in [19] and [20]. The authors of [21] have taken advantage of both current injection and redundancy in their work. They have proposed a current injection with a dual three-phase winding to reduce the torque ripple and to suppress the fault current by field weakening control in case of single phase ITSC. The faulty winding set is used only for fault tolerant control purposes and does not contribute to torque production.

Multiple ITSC fault mitigation techniques including phase terminal shorting, vertical windings, electrical and mechanical shunts were reviewed in [22], [23]. Table I summarizes the

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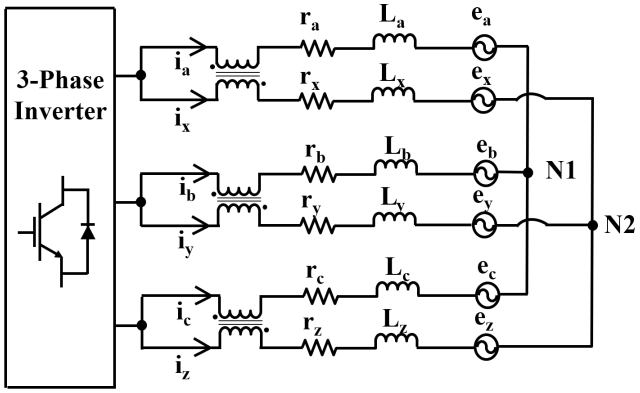

Fig. 1. Equivalent circuit model of the system with the DMCs

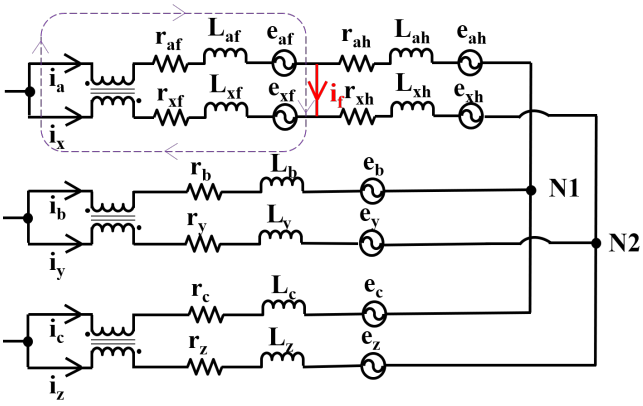

Fig. 2. Equivalent circuit of the motor and DMCs with fault between phases A and X. The gray dashed line indicates the path for Kirchoff's Voltage Law.

comparison in [22], where terminal shorting with the vertical winding was identified as the most effective method for reducing the worst-case fault current. For vertical windings, [24] has shown that the inductance and, consequently, the ITSC current are independent of the position of the shorted turns. However, in more conventional windings, the inductance and ITSC current are highly dependent on the position of the shorted turns, and the worst case is when the fault happens in turns that are located close to the slot opening.

Almost all the proposed methods so far come with some disadvantages. For example, current injection can effectively reduce the fault current, but it increases the copper loss and derates the machine. Additionally, current injection requires knowledge of the fault severity and the machine parameters. Shunting techniques add more weight and cost to the system. Redundancy requires overdesign and increases complexity. Vertical windings have more resistance because turns are wrapped around each other. They also increase eddy current loss and skin effect. Additionally, as shown in Table I, even with these fault mitigation methods, the ITSC fault current may still be larger than the rated current, and the torque will be reduced (unless the current is increased to compensate for the torque reduction, which would increase losses). Finally, any active approach to mitigating ITSC fault currents requires detection of the fault, which can be a significant challenge because the ITSC fault current circulates entirely inside the machine [25].

A new multiphase winding arrangement for form wound coils that can inherently block or reduce short circuit fault currents is proposed in [26]. In this new configuration, ITSC faults become phase to phase faults. Two different types of these faults can happen. For symmetrical faults, the fault happens at the same position in both phases, such as A1-X1 in [26]. On the other hand, for asymmetrical faults, there is an one turn difference in the fault location of the two phases, such as A2-X1 in [26]. For symmetrical faults, the fault current can be reduced to an acceptable level by slightly adjusting the voltage of one of the affected phases. However, for asymmetrical faults, the fault current is significantly larger than for symmetrical faults. Additionally, a 6-phase inverter and active control are required for the voltage adjustment method proposed in [26]. This paper takes the multiphase winding arrangement of [26] and proposes a passive fault current mitigating solution based on adding differential mode chokes (DMCs), which can be implemented with a 3-phase inverter. This method does not require knowledge of the machine parameters or fault severity. Additionally, the proposed method does not require fault detection.

Thus, the proposed approach to mitigate ITSC faults involves two steps. First, we employ a winding arrangement [26] that ensures that faults between adjacent turns in the machine are no longer interturn short-circuit faults but instead become a phase-to-phase faults such that the fault current passes through the machine's terminals. Second, we add the DMCs to reduce the fault current.

TABLE I
COMPARISON OF EXISTING MITIGATION STRATEGIES [22]

Mitigation Strategy	Fault Current (% of rated current)	Torque in Faulted State (% of the rated torque)
Terminal shorting	175%	83%
Current injection	115%	84%
Electrical shunt	141%	67%
Mechanical shunt	141%	84%

II. PROPOSED SOLUTION

Fig. 1 illustrates the equivalent circuit of the model with the DMCs. (Mutual inductances between phases in the machine are not shown here to keep the figure legible.) In healthy operation when there is no fault, i_a and i_x are the same, so the differential mode current is zero. Thus, in the healthy situation, an ideal DMC does not have any effect on the system. However, in practice, DMCs have a small leakage inductance and a small resistance which slightly increases the required voltage and the losses. Fig. 2 shows the equivalent circuit in the case of a short circuit fault between phases A and X. The fault current manifests itself as a differential mode current between the two affected phases (A and X in this example). Thus, the fault current can be reduced by increasing the differential mode impedance, which is the purpose of the DMCs. Applying Kirchhoff's Voltage Law (KVL) around the

dashed gray fault loop of Fig. 2 yields

$$\begin{aligned} &j\omega L_s i_a - j\omega L_m i_x + r_c i_a \\ &+r_{af} i_a + j\omega L_{af} i_a + j\omega L_{af,ah}(i_a - i_f) \\ &+j\omega L_{af,xf} i_x + j\omega L_{af,xh}(i_x + i_f) + e_{af} - e_{xf} \\ &-j\omega L_{xf} i_x - j\omega L_{af,xf} i_a - j\omega L_{xf,ah}(i_a - i_f) \\ &-j\omega L_{xf,xh}(i_x + i_f) - r_{xf} i_x \\ &+j\omega L_m i_a - j\omega L_s i_x - r_c i_x = 0 \end{aligned} \tag{1}$$

where L_s and L_m are self and mutual inductances of the DMC, respectively, r_c is the resistance of the DMC, and $L_{af,ah}$, $L_{af,xh}$, $L_{af,xf}$, $L_{xf,xh}$, and $L_{xf,ah}$ are the mutual inductances. This assumes that the mutual inductances with the other phases are negligible as is often the case for fractional slot concentrated windings (FSCW) [27]. Rearranging (1) in terms of common mode (i_{cm}) and differential mode (i_{dm}) currents where

$$i_a = i_{cm} + i_{dm} \tag{2}$$

$$i_x = i_{cm} - i_{dm} \tag{3}$$

yields

$$\begin{aligned} &i_{cm}\Big((r_{af} - r_{xf}) + j\omega(L_{af} - L_{xf}) + \\ &j\omega(L_{af,ah} - L_{xf,ah}) + j\omega(L_{af,xh} - L_{xf,xh})\Big) \\ &+i_{dm}\Big(2(j\omega L_s + j\omega L_m + r_c) + (r_{af} + r_{xf}) + \\ &j\omega(L_{af} + L_{xf}) + j\omega(L_{af,ah} - L_{xf,ah}) \\ &-2j\omega L_{af,xf} - j\omega(L_{af,xh} - L_{xf,xh})\Big) \\ &+i_f\Big(j\omega(L_{af,xh} - L_{af,ah} + L_{xf,ah} - L_{xf,xh})\Big) \\ &+e_{af} - e_{xf} = 0 \end{aligned} \tag{4}$$

Based on Fig. 2, in the faulty condition, the fault current results in differential mode currents between the phase pairs (A and X, B and Y, C and Z). The self and mutual inductances of the DMC introduce a differential mode impedance in the fault loop in (4), which reduces the fault current. The level of fault current reduction depends on the DMC size. This method provides a simple approach to ITSC fault tolerance without many of the drawbacks of other approaches, such as complicated control algorithms, dependence of knowledge of the fault severity and machine parameters, or the need for a multiphase inverter.

Like any other method, this solution has its own disadvantages and constrains. For example, the leakage inductance and resistance of the DMCs do slightly affect healthy operation. Also, the DMCs add a small weight which affects the power density of the system; however, they could potentially be integrated into the stator laminations to minimize the added part count. Additionally, the proposed winding arrangement is only applicable to machines with form-wound windings, where the location of each turn in the slot is known. Finally, the proposed solution increases the complexity of the winding arrangement and requires two separate neutral points.

III. Simulation Analysis

The proposed solution is implemented in finite element analysis (FEA) on a SPM motor. Fig. 3 shows a cross section of the motor with the winding arrangement in a slot. The parameters of the motors are given in Table II. The studied motor has 12 slots and 10 poles and utilizes a FSCW. In this arrangement the mutual inductances between phases in different slots are negligible. In this paper, we have considered FSCW arrangement since these avoid overlapping end turns, which would provide additional opportunities for faults. While most FSCW machines are random wound, they can be form wound, particularly for high performance applications where power density and thermal performance are critical [1], [28]–[31].

The fault current is highly dependent on the self and mutual inductances of the individual turns and the harmonic components of the back emf. Thus, FEA was used to determine these machine parameters. Windings A and X were divided into a faulty section (including the turns between the short circuit and the inverter) and a healthy section (between the short circuit and the neutral point). Based on the fault case scenario, the number of turns for the faulty and healthy sections of the windings were assigned. Then, machine parameters including self and mutual inductances of the all windings and back emfs were extracted and plugged into the developed Simulink model illustrated in Fig. 4 to analyze different fault scenarios with different DMCs. (While an analytical model based on the equivalent circuit could be used for the fault current, instead of the Simulink model, it would need to be evaluated for each different harmonic component of the back emf and for each switching harmonic to determine the fault current.) By removing or adding the fault connection, the healthy or faulty cases can be simulated. With the developed Simulink model, different healthy, symmetrical fault, and asymmetrical fault cases with different DMC inductances can be evaluated quickly.

A. Asymmetrical without DMC

Fig. 5 illustrates the A_f, X_f and fault currents in case of an A2-X1 asymmetrical fault. Fig.5 shows that the A_f and X_f currents are largely out of phase due to large fault current. Thus, the differential mode current is much larger than the common mode current. The fault current has a RMS of 2362 A, which is 4586% of the nominal current. This much fault current passing through the windings is hazardous and could cause catastrophes like fire. In addition, the fault current causes torque ripple. Fig. 6 shows the torque waveforms in healthy and the A2-X1 fault conditions. In this case, the torque ripple is increased from 37% to 59% of the average torque. The average of the torque is also decreased by 15.5%.

B. Asymmetrical with DMC

Adding a DMC can significantly reduce the fault current. This is a passive and robust solution that does not require

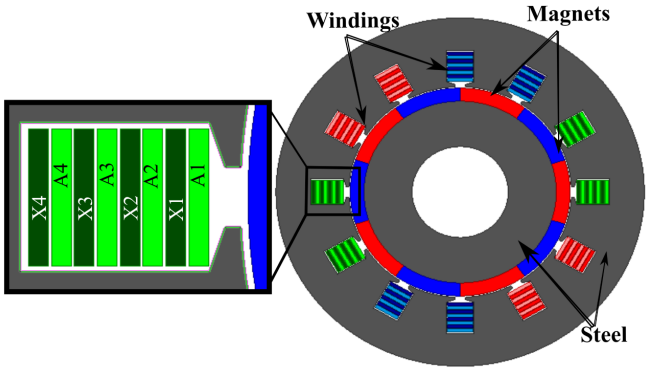

Fig. 3. Example motor with the proposed winding arrangement in [26]

TABLE II
PARAMETERS OF THE SIMULATED MOTOR

Parameters	Value	Unit
Outer/inner diameter of stator	134/81	mm
Outer/inner diameter of rotor	80/35	mm
PM thickness	5	mm
Core stack length	100	mm
Air gap length	0.5	mm
Stator slot opening depth/width	1/4	mm
Stator slot depth/width	12/10	mm
Number of stator slots	12	-
Conductor cross sectional area	11.5	mm^2
Nominal operating conditions for the simulated motor		
Average output torque	18.0	Nm
Rotational speed	6000	rpm
RMS phase voltage	37.8	V
RMS phase current	51.5	A
Fundamental Frequency	500	Hz
Switching Frequency	16.5	kHz

any complex active control algorithm or even detection of the fault. As stated before, the fault current results in a differential current between A and X. In this case, the DMC reduces the fault current to an extent depending on the choke size by introducing a differential mode impedance in the fault loop (4). Fig. 7 shows the fault current and A_f and X_f currents after adding a DMC with the same inductance as each phase, which is 17.92 μH. The RMS of the fault current is reduced from 2362 A (4586% of the nominal current) to 64.7 A (125.6% of the nominal current). In addition, the A_f and X_f currents are much more in-phase compared to the no DMC case. It is worth mentioning that unlike inductors, chokes do not generally store magnetic energy, so they don't usually have any air gap. Therefore, a DMC can be much smaller than an inductor with a similar inductance.

While the DMC does significantly reduce the fault current, the fault current is still larger than the nominal current and may generate significant heat. Therefore, the DMC should be sized to reduce the fault current to a level such that the machine can continue to operate safely. Fig. 8 shows the effect of different DMC sizes on the fault current. As can be seen, the fault current is reduced by multiple orders of magnitude. Based on Fig. 8, adding a 200 μH DMC can decrease the fault current to 5 A (10% of the rated current). With the DMC, the fault current is primarily on the d-axis which is orthogonal to the normal current. Thus, a fault current that is 10% of the nominal current, increases losses in the affected turns by only 1%. With this level of mitigation, the machine can continue operation with a minimal increase in risk of further faults developing.

C. Symmetrical

As discussed before, the other type of fault, the symmetrical fault, is where the fault happens at the same position in both affected phases. The A1-X1 symmetrical fault is analyzed here as the worst case symmetrical fault [26]. Unlike the asymmetrical type, the symmetrical fault current is not as dangerously high. In this case as shown in Fig. 9, the fault current, when there are no DMCs, is 66.2 A or 128% of the nominal current. Fig. 8 shows the effect of DMC inductance on the fault current for A1-X1 case, as well. As can be seen, a 20 μH DMC decreases the fault current by more than two orders of magnitude to less than 1% of the rated current. Thus, the DMC should be sized for the asymmetrical fault.

D. DMC sizing approach

The DMC inductance can be chosen based on the worst-case scenario, which we know is the asymmetrical A2-X1 fault. (Symmetrical faults yield much lower currents than asymmetrical faults, and including more turns in the fault current loop increases the resistance of the fault current loop, reducing the fault current.) Varying the DMC inductance in the Simulink model will yield a curve like that shown in Fig. 8, which can be used to select the size of the inductance based on how much fault current is thermally tolerable for a given machine and application. The fault current in Fig. 8 tends to be inversely proportional to the DMC inductance above very small values of DMC inductance (because the impedance of the DMC dominates the impedance of the fault current loop inside the machine); thus, the curve could be reasonably predicted from just a few simulated DMC inductance values. Additionally, the resistance of the DMC winding adds copper loss, which might have an impact on the efficiency of the system. As an example, using a commercially available DMC (Part number RB6522-50-0M3 from manufacturer Shaffner EMC, Inc.) with a resistance of 0.9 mΩ and an inductance of 250 μH, would increase copper losses at nominal operation by 14.3 W, causing the efficiency to decrease by 0.1%. Thus, the impact of the DMCs on efficiency is generally expected to be relatively small.

IV. EXPERIMENTAL ANALYSIS

A. Setup description

An experimental setup was built and tested to validate the proposed method for mitigating the fault current. In order to have a safe and simpler experiment, the test was implemented on transformer cores, instead of a SPM machine. In the SPM machine, the PM excitation cannot be turned off immediately if something goes wrong during the experiment, which can be dangerous. In addition, with the transformer cores, the windings are more accessible for rewinding and testing different scenarios. The mutual inductance between windings in different cores is insignificant, which is similar to the phases of a FSCW SPM machine. Fig. 10 shows the experimental setup. The proposed winding arrangement in

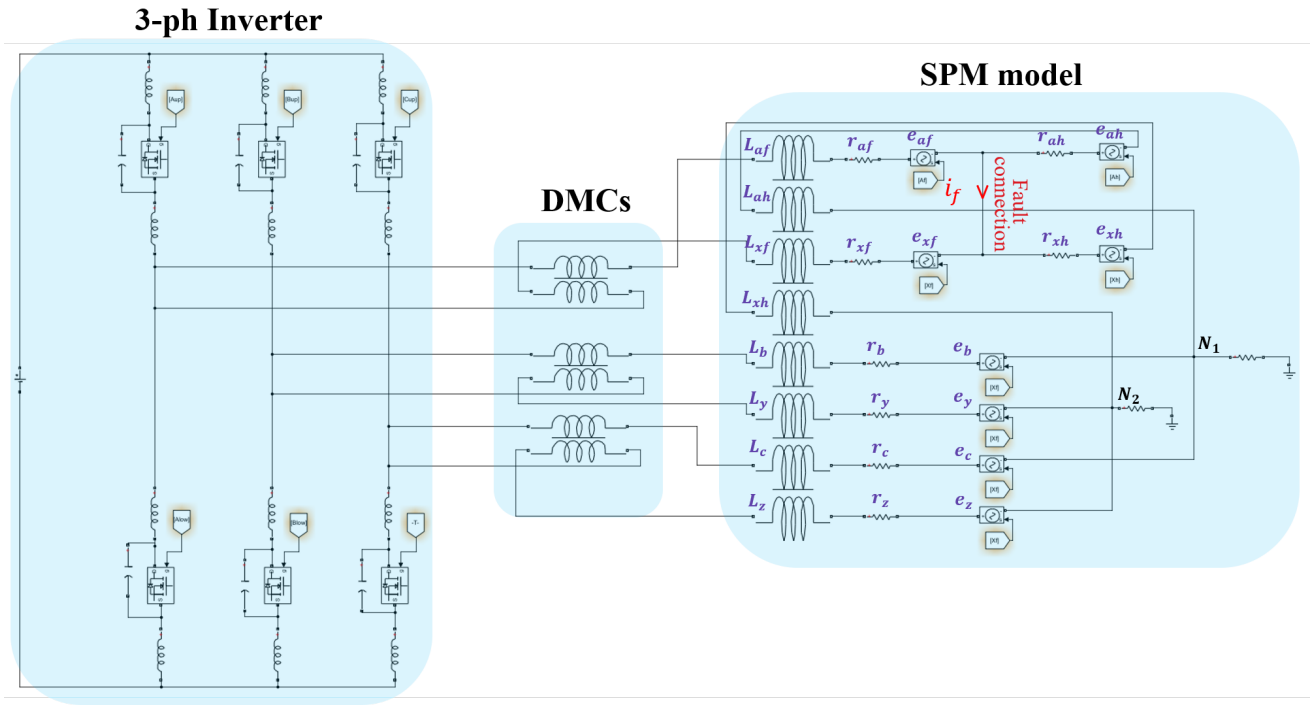

Fig. 4. Simulink model for the studied SPM motor

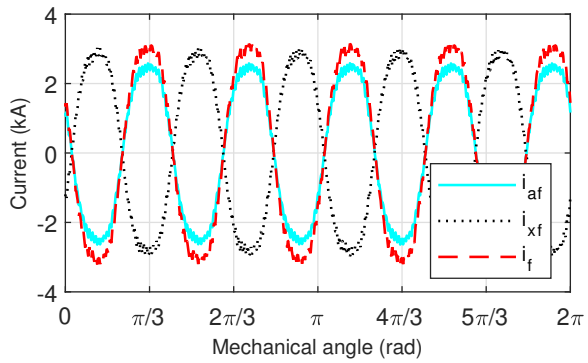

Fig. 5. Winding A_f, winding X_f, and fault currents in case of A2-X1 fault

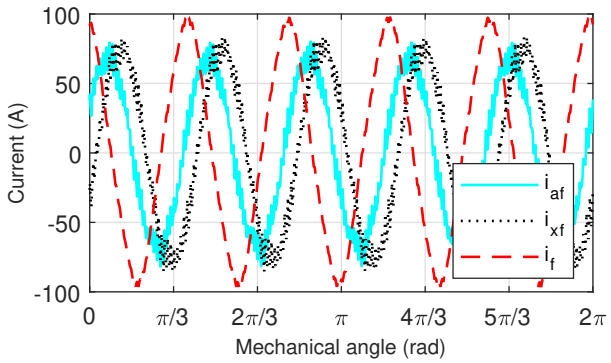

Fig. 7. Winding A_f, winding X_f, and fault current in case of A2-X1 fault with 17.92 μH DMCs

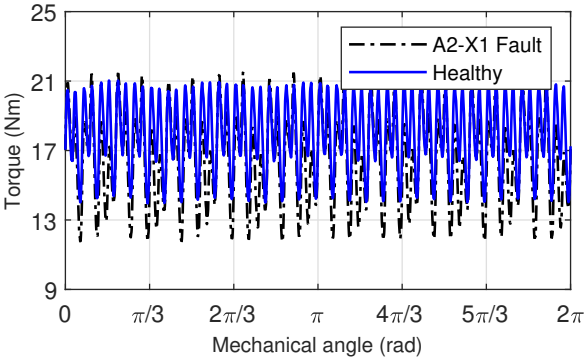

Fig. 6. Torque waveforms in healthy and A2-X1 faulted case

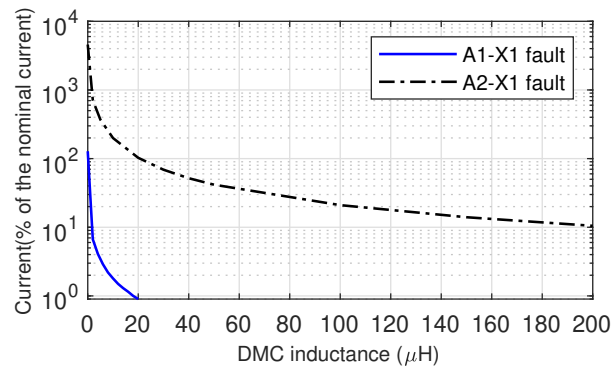

Fig. 8. Effect of different DMC size on the fault current

[26] is implemented on 6 transformer cores. Each phase pair utilizes two cores to alternate the turn locations to have the same inductance in each phase, as shown in Fig. 11. This is analogous to Fig. 3 where there are two coils for each phase pair and the positions of the phases are transposed between coils. The A-X phase pair was sectioned to create a non-invasive removable fault outside of the core. In Fig. 10, the current probe is measuring the fault current. Tests were

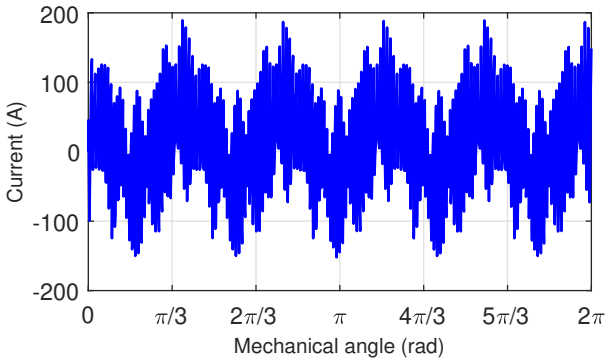

Fig. 9. A1-X1 fault current without DMCs

initially performed with the DMCs disconnected, as shown in Fig. 10. Then tests were performed with the DMCs connected between the inverter and the transformers. The inductances of the DMCs were varied by changing the airgap thickness and the number of turns to characterize the impact of the DMC impedance on the fault current. Fig. 12 shows the equivalent circuit of the experimental setup. For each of the 6 transformers, the secondary coil has 20 turns and each of the two primary coils has 4 turns. Thus, each of the two cores in Fig. 11 has 4 turns for phase B, 4 turns for phase Y, and 20 turns for the secondary. These are connected in series such that phase B has a total of 8 turns, phase Y has a total of 8 turns, and the secondary has a total of 40 turns. The 3-phase load is connected to the secondary to dissipate the power. In this setup, the secondary is included so that power is transferred through the airgap. DMCs were built with the similar cores as the transformers. In order to achieve different DMC inductances, the airgap length and number of turns of the DMCs were varied to reach a wide range of inductances. For changing the airgap length, small plastic sheets with different thicknesses (0.1 mm steps) were 3-D printed. With these two degrees of freedom (airgap length and number of turns), DMC inductances of 0.6 μH, 2.6 μH, 4.6 μH, 6.6 μH, 8 μH, 12.5 μH, 16.4 μH, 25 μH, and 65 μH were achieved. Table III shows the winding parameters that were measured with an Applent AT2817A digital LCR meter. L_a, L_x, L_b, L_y, L_c, and L_z are the self inductances of each phase in the healthy condition. Similarly, $L_{s,p}$ is the healthy mutual inductance between a secondary and a primary phase. Likewise, $L_{a,x}$, $L_{b,y}$ and $L_{c,z}$ are mutual inductances between phase pairs in healthy condition. The inductances and resistances in the faulty condition depend on the location of the fault. Other specifications of the experimental setup are given in Table IV. A Simulink model based on these parameters was developed for comparison against the experimental results. Fig. 13 shows the annotated Simulink model of the experimental setup. The experimental results are compared and verified against this model.

B. Results and discussion

Fig. 14 shows the currents in Phases A and X in the healthy case without the DMCs. As expected, the currents in a and x are almost identical. Before applying any fault, the nominal

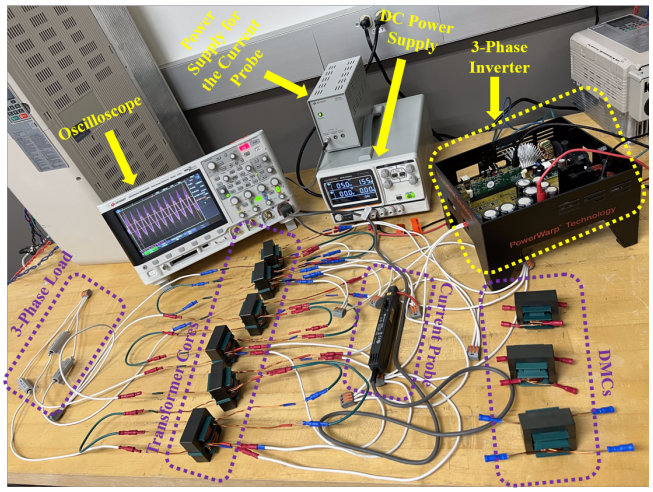

Fig. 10. Experimental setup

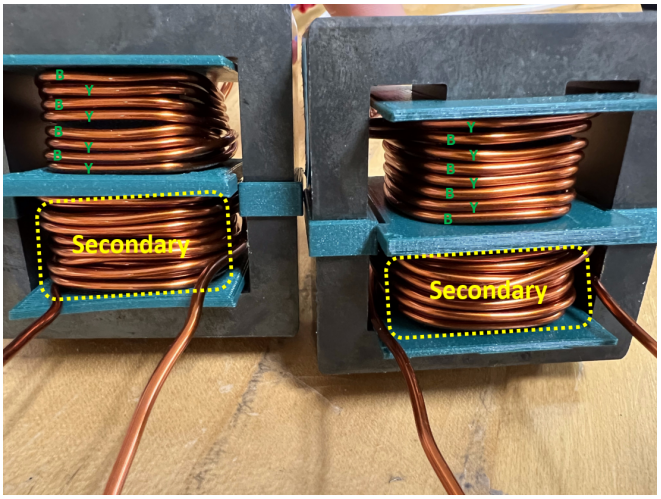

Fig. 11. Two cores with transposed coils for each phase pair

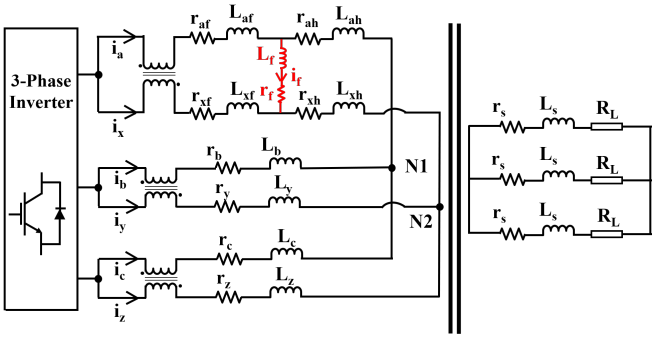

Fig. 12. Equivalent circuit of the experimental setup with the DMCs with fault between Phases A and X

current was measured for healthy case with different DMC sizes added to the phase pairs. With 2.6 μH DMC, the RMS of the healthy current decreased to 1.12 A, which is 2.6% less than the nominal current for the healthy case without any DMC, as reported in Table IV. Adding a 65 μH DMC decreased the RMS of the healthy current to 1.08 A or 6% less than the nominal current without any DMCs. As mentioned in

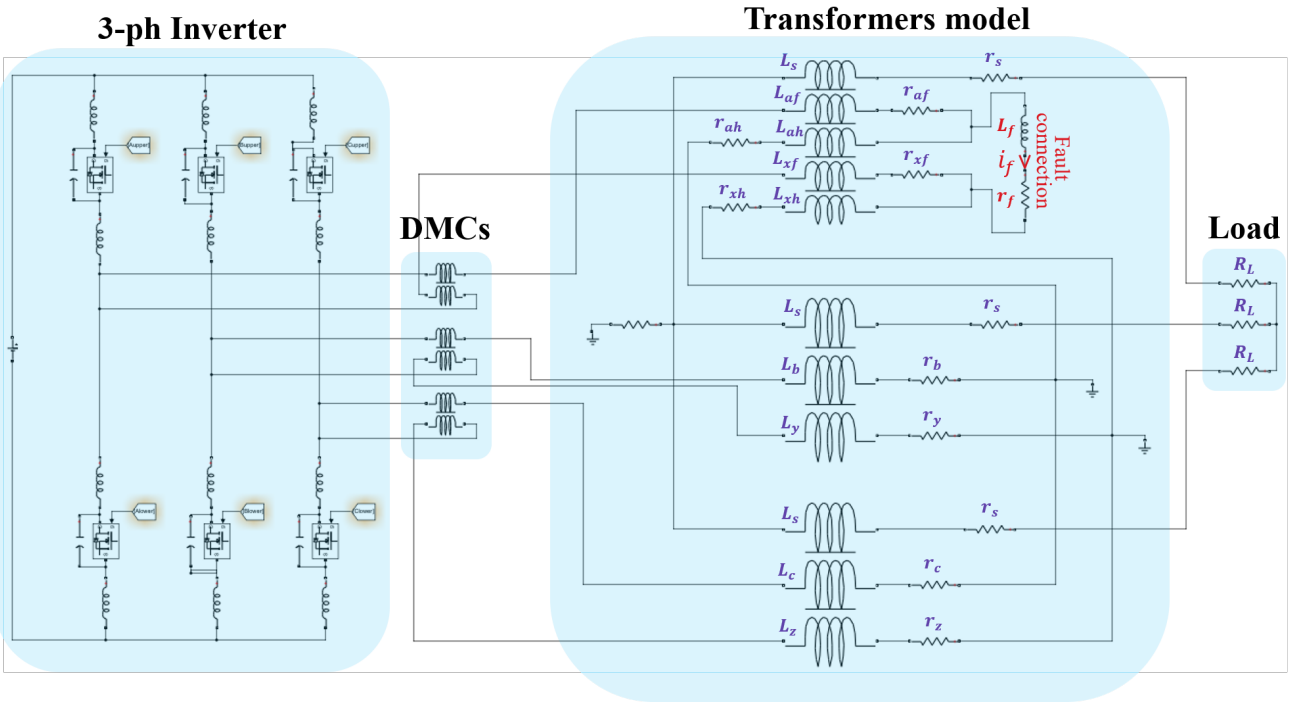

Fig. 13. Simulink model for the experimental setup

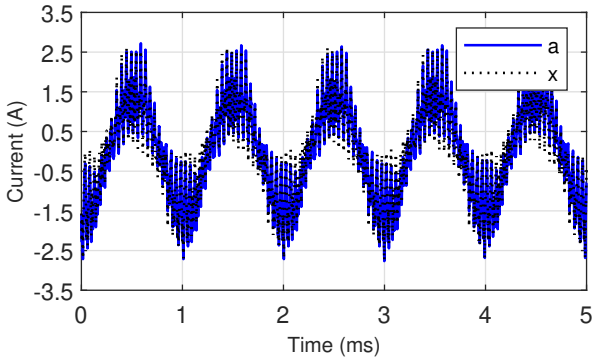

Fig. 14. Currents in phases A and X in the healthy case without DMCs

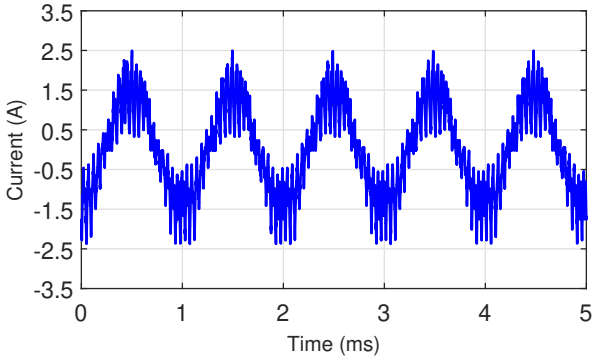

Fig. 15. Current in phase A in the healthy case with a 65 μH DMC

the proposed solution section, this minor reduction in healthy current was expected since DMCs have a small resistance and leakage inductance which slightly increase by increasing the DMC size. Thus, the required voltage would need to be

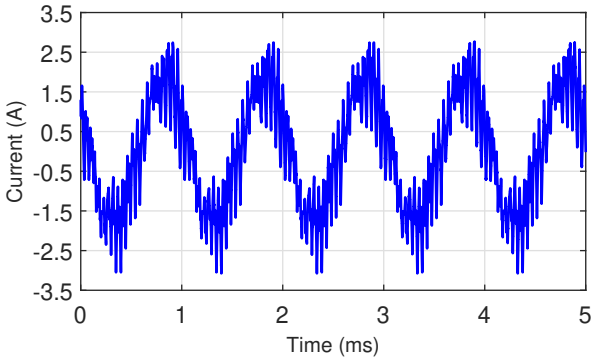

Fig. 16. A2-X1 fault current without DMCs

TABLE III
WINDING PARAMETERS OF THE EXPERIMENTAL SETUP

Parameters	Value	Unit
$r_a = r_x = r_b = r_y = r_c = r_z$	10	mΩ
r_s	43	mΩ
L_s	490	μH
$L_a = L_x = L_b = L_y = L_c = L_z$	23	μH
$L_{s,p}$	91	μH
$L_{a,x} = L_{b,y} = L_{c,z}$	22	μH
L_f	0.74	μH
r_f	7.3	mΩ

TABLE IV
EXPERIMENTAL SETUP SPECIFICATIONS

Parameters	Value	Unit
DC bus voltage	5	V
Rated current	1.15	A
Switching frequency	21	kHz
Fundamental frequency	1	kHz
Load resistance	6.8	Ω

slightly increased to have the same nominal current as the case without any DMC. Fig. 15 shows the Phase A nominal current

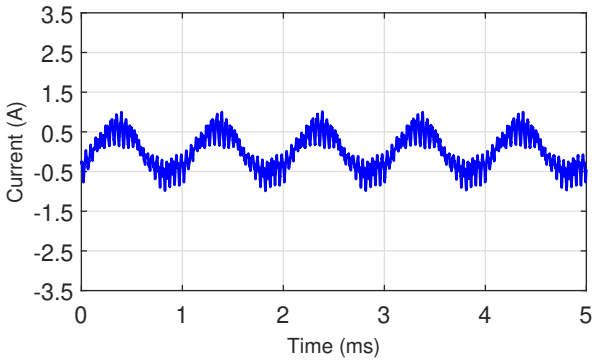

Fig. 17. A2-X1 fault current with 2.6 μH DMC

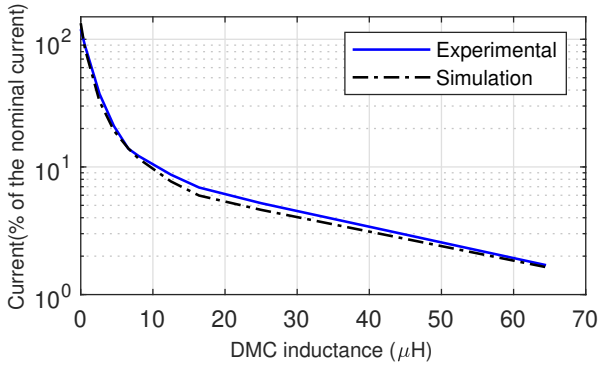

Fig. 18. Effect of different DMC sizes on the fault current for the A2-X1 faulted case

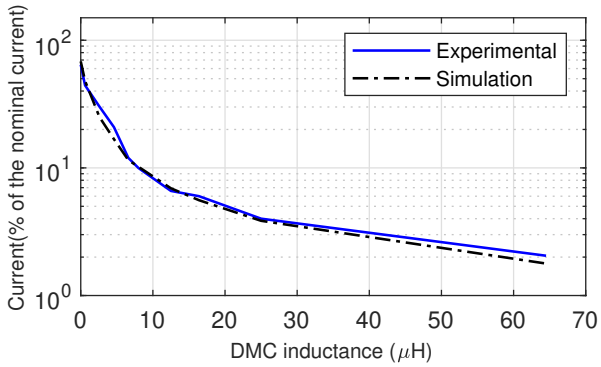

Fig. 19. Effect of different DMC sizes on the fault current for the A6-X5 faulted case

with 65 μH DMC added to the phase pairs. An asymmetrical A2-X1 fault was then applied between the second turn of A and first turn of X. Fig. 16 illustrates the fault current in the A2-X1 faulted case without DMCs. The RMS of the fault current was 1.38 A or 120% of the rated current. 2.6 μH inductance DMCs were added between the inverter and the transformers to see their effect on the fault current. The fault current was decreased to 0.43 A RMS or 37.3% of the rated current, as shown in Fig. 17. Fig. 18 shows the effect of the DMC size on the fault current for the A2-X1 faulted case. A 10μH DMC can decrease the fault current more than an order of magnitude to 10% of the rated current. With a 65μH DMC, the fault current is as low as 1.6% of the rated current which is almost two orders of magnitude smaller than the initial fault current without DMC.

Considering (4), increasing the numbers of turns between the inverter and the fault will have minimal effect on the net inductance for the differential mode current and on the net emf in the KVL path, but it will increase the resistance for the differential mode current. Therefore, the fault current in A6-X5 case is smaller than in the A2-X1 case. The fault current in the A6-X5 faulted case without DMCs is 0.74 A or 64% percent of the rated current which is about half of the fault current in A2-X1 case. Fig. 19 shows the effect of the DMC size on the fault current for the A6-X5 faulted case. The initial fault current without DMCs and fault currents with smaller DMCs ($<$15μH) are different for the A2-X1 and the A6-X5 cases. However, for larger DMCs ($>$15μH), the fault currents for both cases tend to be similar. This occurs because, for larger DMCs, the inductance of the DMCs dominates the difference in resistances between the A6-X5 and A2-X1 cases. In both asymmetrical faulted cases, the good agreement between the experimental and simulation data shows the legitimacy of the analysis.

Fig. 20 shows the A1-X1 fault current without DMC. In this case, the fault path contains the same number of turns in phases A and X. However, because the locations of the turns in the slot are different, their inductances are slightly different. Thus, a small fault current is still produced. In this case, the rms of the fault current is 0.113 A or 9.8% of the rated current without any DMCs. Thus, the DMC size should be based on the A2-X1 fault case rather than the A1-X1 fault case.

V. Conclusion

In this paper a passive mitigation technique for short circuit faults was proposed to build on the multiphase winding arrangement presented in [26]. The fault current manifests itself as a differential mode current between the affected phases. Thus, a method based on adding the DMCs between the inverter and phase pairs was proposed. The DMCs only slightly affect the normal operation of the machine. A Simulink model for a PMSM was developed based on the parameters extracted from a FEA model. It was shown that the largest fault current results from a short between the second turn of one phase and the first turn of its paired phase. In this worst case, the fault current was reduced from 4586% without DMCs to less than 10% of the rated current with 200 μH DMCs. Thus, with the proposed passive mitigation scheme, the machine can continue operating almost normally in the presence of a single fault. In another fault scenario, the fault current was reduced to less than 1% of the rated current with the same size DMCs. Therefore, the DMCs should be sized based on the worst faulted case.

An experimental setup based on transformer cores was built and tested. The test results confirmed which case produced the largest fault current. In that case the fault current was reduced from 120% to less than 1% of the rated current with 65 μH DMCs. The simulation and experimental results showed a sound agreement which validated the model.

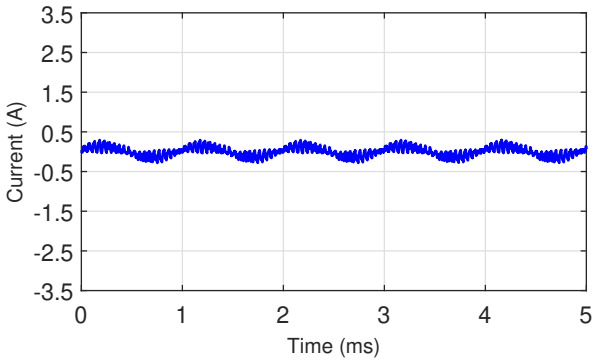

Fig. 20. A1-X1 fault current without DMCs

VI. Acknowledgement

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